

Excitability in autonomous Boolean networks

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Abstract – We demonstrate theoretically and experimentally that excitable systems can be built with autonomous Boolean networks. Their experimental implementation is realized with asynchronous logic gates on a reconfigurable chip. When these excitable systems are assembled into time-delay networks, their dynamics display nanosecond time-scale spike synchronization patterns that are controllable in period and phase.

Introduction. – Excitability is a property of dynamical systems, where the system rests in a stable fixed point, but large excursions in phase space (*spikes*) can be generated in response to small perturbations above a threshold [1]. When coupled in networks, excitable systems can exhibit complex spatio-temporal spike patterns and synchronized oscillations as observed in chemical reactions [2], heart tissue [3], and populations of interacting neurons [4, 5]. This abundance of excitability in nature has motivated many theoretical and experimental studies.

Theoretical approaches, such as the paradigmatic model for excitability proposed by FitzHugh and Nagumo [6, 7], have helped to uncover and understand the diverse collective behaviors (bursting, cluster synchronization, and phase transitions, for example) that arise in networks of excitable systems [8–12]. However, they usually do not fully integrate all experimental imperfections and heterogeneities like noise and system parameter variation, which may have significant impact on the dynamics.

This motivates experimental studies on excitable systems, for example, with analog electronic circuits. These electronic systems can be realized in very large scale integration (VLSI), where up to thousand excitable systems are implemented on a custom analog chip and the coupling topology is handled by a separate reconfigurable digital chip [13, 14]. This configuration, however, presents major hindrances due to speed limitations, the cost and long design cycle time of the custom analog chip, and its connections to the digital reconfigurable chip. Of particular concern is the fact that the analog signal is digitized, leading to discretization errors in the coupling.

To address these issues, we propose an excitable system built from continuous-time asynchronous logic gates. This system is based on autonomous time-delay Boolean networks that have been found previously to show oscillatory dynamics and chaos depending on the choice of topology and Boolean functions [15–20]. With our approach, we can experimentally realize the excitable systems and couple them to networks on a single inexpensive field-programmable gate array (FPGA).

The resulting dynamics are spike synchronization patterns reproducible with a theoretical Boolean map. They are controllable by the network’s link delay times [21] and are much faster than the dynamics of common networks of excitable systems. The nanosecond timescales give our approach an advantage for potential ultra-fast neuro-inspired data processing [22], similar to reservoir computing [23].

Experimental setup. – Our design realizes three important properties characterizing excitability [1]: (i) the all-or-none principle, where the system responds only if an input is above a threshold and stays quiescent otherwise; (ii) pulse dynamics, where output pulses have fixed width independent of the input pulse shape; and (iii) a refractory phase, where the excitable system remains unresponsive during a refractory period after generating an output pulse.

Asynchronous logic gates are well suited to fulfill these properties. The all-or-none principle (i) is intrinsically embedded in logic gates [24]. Their output voltages V transition between $V = V_{\text{high}}$ (the *high* level) and $V = V_{\text{low}}$ (the *low* level) as their inputs cross a threshold V_{th} . Pulse dynamics (ii) and the refractory phase (iii) can be realized through pulse generators (PGs), which exploit the

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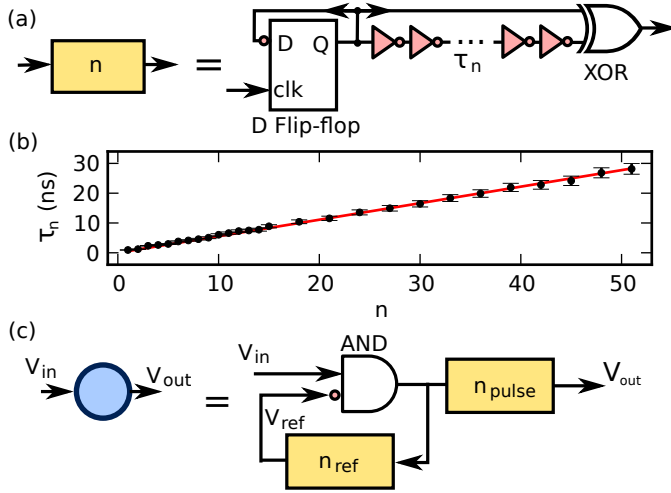


Fig. 1: (Color online) (a) Setup of the pulse generator (PG) characterized by an integer n , which represents the number of pairs of inverters in the delay line and thus its time delay $\tau_n \sim 2n\tau_{\text{gate}}$. The pairs of inverters act as time delays that do not change the Boolean state. (b) Experimental measurement of the delay time τ_n comprising n pairs of inverter gates, with relative error of $\sim \pm 3.5\%$ (error bars) and linear regression (red line) with $\tau_n \sim 2n \cdot 280$ ps. (c) Complete design of an excitable node; it combines one pulse generator labeled n_{pulse} to realize the pulse dynamics with another one labeled n_{ref} to realize the refractory phase. The refractory period of the excitable system T_{ref} and its pulse width T_{pulse} are determined by the integers n_{ref} and n_{pulse} , respectively. The voltages V_{in} and V_{ref} are inputs to an AND gate, where the second input is inverted, as indicated by a circle.

intrinsic propagation delays of logic gates τ_{gate} .

As shown in Fig. 1a, the PG is implemented using a D-type flip-flop, a delay line of duration $\sim \tau_n$ made of $2n$ inverters with $n \in \mathbb{N}$, and an asynchronous logic gate executing the XOR operation [25]. Its dynamics consists of the generation of a single pulse of width T_n in response to a positive edge (low to high transition). More specifically, in response to a positive edge at its clock (clk) input, the flip-flop with connection from output (Q) to inverted input (D) generates a Boolean transition at its output (Q). This signal reaches the XOR gate inputs with a time-delay difference $\sim \tau_n$, due to a delay line. As a consequence, the XOR gate has different input logic values during the time delay and hence generates a high voltage V_{high} of width $T_n = \tau_n \propto n$, with delay τ_n measured in Fig. 1b.

We combine two PGs with an AND gate, as depicted in Fig. 1c, so that the system exhibits excitable dynamics in its output voltage V_{out} in response to an above-threshold input voltage V_{in} . The PG labeled n_{pulse} (n_{ref}) produces a voltage pulse V_{pulse} (V_{ref}) of width T_{pulse} (T_{ref}). The voltage V_{ref} indicates whether or not the system is in its refractory phase (V_{ref} high or low, respectively); its interplay with V_{in} governs the dynamics of our excitable node.

When V_{ref} is low and V_{in} has a positive edge, the AND gate also generates a positive edge so that each PG pro-

duces a pulse. V_{pulse} is sent to the output of the excitable system and the high value of V_{ref} now blocks inputs V_{in} to the AND gate for the refractory period T_{ref} and, therefore, prevents pulse generation during that time. When the refractory phase ends, *i.e.*, V_{ref} is back to a low voltage, the system becomes responsive to input excitations V_{in} again.

Our design of the excitable node is motivated by the dynamics of integrate-and-fire neurons [26], where the membrane potential evolves as a function of its synaptic input. When inputs are present, the membrane potential increases (integration) until it reaches a threshold, the condition for generating a pulse (firing). In our approach, in contrast, the excitable system compares its input voltage directly to a threshold without an electronic analog of a membrane potential. Consequently, when increasing V_{in} above the threshold of our system, oscillations start with a constant (finite) period, so that our system exhibits a behavior analogous to type-II excitability [1]. After generating a pulse, the membrane potential of integrate-and-fire neurons returns to a resting value and its dynamics is deactivated for a finite duration [26], which is the same mechanism used in our system to realize a refractory period.

The implementation of our system can be realized with various technologies. Here, we use an FPGA because of the very large number of logic elements and flip-flops available (up to $\sim 10^6$ [27]) and the possibility to operate them asynchronously. Another advantage of FPGAs is the reprogrammability of the logic elements. They consist of CMOS-based multiplexers fed by rewritable memory bits with a specific arrangement to realize the logic gate operation. These multiplexers connect N inputs ($N = 4$ for the FPGA used here) to one output so that the overall behavior is that of a logic gate with the same operation. Finally, FPGAs ensure flexible connection of logic elements [27], allowing us to realize large networks of excitable elements.

Dynamics of one excitable node. — In this section, we conduct experiments on a single excitable node driven first by a constant input and second by self-feedback, constituting a simple network. The experiments are realized on an Altera Cyclone IV FPGA (EP4CE115F29C7N), which has $\sim 115,000$ logic elements with propagation time delay and rise time of $\tau_{\text{gate}} = (280 \pm 10)$ ps and $\tau_{\text{rise}} = (310 \pm 10)$ ps, respectively. Signals generated within the FPGA pass through an additional input-output logic gate (hardwired to the output pins of the FPGA) before being acquired by a high-speed oscilloscope (DSO80804A) with 8 GHz bandwidth and 40 GSa/s sampling rate.

We apply a constant, above-threshold input voltage V_{in} to the excitable node (Fig. 2a). In response, it generates periodic pulses with width of a few nanoseconds, as shown in Fig. 2b. In this regime, the system is oscillatory, similar to biological neurons with constant stimulus [1]. To understand the dynamics, we analyze the output voltage V_{out} and the voltage V_{ref} that indicates the refractory phase.

The pulses in V_{out} and V_{ref} are generated almost simul-

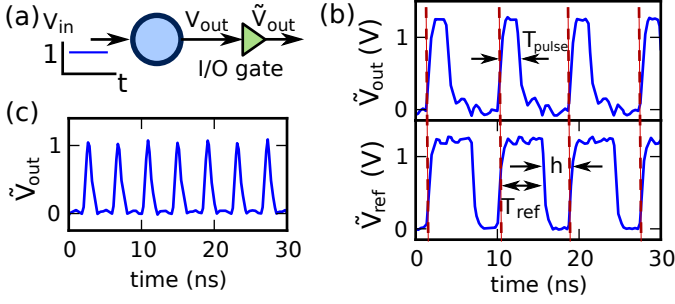


Fig. 2: (Color online) (a) An excitable node on the FPGA is subject to a constant above-threshold input voltage V_{in} . The output voltage V_{out} and V_{ref} pass input-output (I/O) gates with outputs labeled \tilde{V}_{out} and \tilde{V}_{ref} , respectively. (b) Both voltages are recorded for $T_{ref} = (5.40 \pm 0.05)$ ns ($n_{ref} = 10$), $T_{pulse} = (2.34 \pm 0.05)$ ns ($n_{pulse} = 4$). (c) Output \tilde{V}_{out} of a minimal implementation of the excitable node with $T_{ref} = (0.68 \pm 0.04)$ ns ($n_{ref} = 1$), $T_{pulse} = (0.80 \pm 0.04)$ ns ($n_{pulse} = 1$).

taneously at times indicated by vertical dashed lines in Fig. 2b. The pulse in V_{ref} indicates the refractory phase and its pulse width equals the refractory period. Therefore, the refractory phase starts at the dashed lines and ends when V_{ref} is low. Then, the system generates a new pulse, which is induced by a negative edge transition in V_{ref} , since $V_{in} > V_{th}$. It requires an additional processing time h to generate the output pulse, which is due to the flip-flops in the PGs and is measured to be $h = (3.2 \pm 0.4)$ ns. This processing time, together with the refractory period T_{ref} , constitutes the period of the pulses in this experiment ($T = T_{ref} + h$). The pulse width in V_{out} is given by T_{pulse} .

The dynamics is determined by T_{ref} , which accounts for the period of oscillations, and T_{pulse} , which determines the width of output pulses of the system; these two quantities are controlled by parameters n_{ref} and n_{pulse} , respectively, as shown in Fig. 1b: $T_{ref} \approx 2n_{ref}\tau_{gate}$ and $T_{pulse} \approx 2n_{pulse}\tau_{gate}$, as follows from the construction shown in Fig. 1a. This can be seen experimentally when conducting the same experiment with different parameters n_{pulse} and n_{ref} . For example, with $n_{pulse} = n_{ref} = 1$, which constitutes a minimal number of seven logic gates, the pulse widths T_{pulse} are on a sub-nanosecond scale and the period T is dominated by h (Fig. 2c).

Experimental fluctuations in T_{ref} and T_{pulse} are characterized in two ways. First, when comparing different measurements of T_{ref} and T_{pulse} on a single implementation, we obtain temporal fluctuations of $\pm 1\%$, with an origin described in the next paragraph. Second, when comparing the measurements of T_{ref} and T_{pulse} on several different copies of the same excitable node on the same chip, we obtain a significantly larger error of $\pm 3.5\%$. The origin of this error is heterogeneity in the propagation delays from logic element to logic element.

Finally, the dynamics of the excitable system is analog-like and fluctuates in pulse shape and timing. These non-

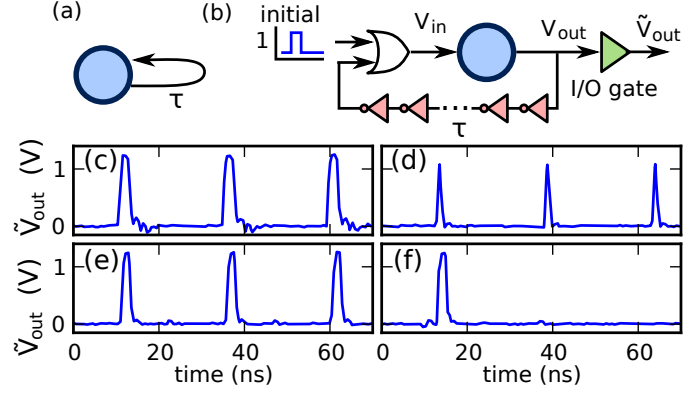


Fig. 3: (Color online) (a) Scheme of one excitable node with delayed feedback where the delayed feedback link is represented as an arrow. (b) Representation of (a) with logic elements used for the feedback. The pink triangles with circles represent 80 inverter gates that are incorporated to implement a time delay of $\tau = (21.3 \pm 0.5)$ ns ($n_{\tau} = 40$). (c),(d) Resulting dynamics with parameters as in Fig. 2(b) and (c), respectively. (e) Same with $T_{ref} = (10.75 \pm 0.05)$ ns ($n_{ref} = 20$), $T_{pulse} = (1.95 \pm 0.03)$ ns ($n_{pulse} = 4$). (f) Same with $T_{ref} = (24.04 \pm 0.05)$ ns ($n_{ref} = 45$), $T_{pulse} = (2.05 \pm 0.05)$ ns ($n_{pulse} = 4$).

ideal experimental behaviors originate from low pass filtering, jitter, and history- and state-dependency of the propagation time delays within logic gates [16, 28]. The asynchronous logic operation is limited in speed only by the high-frequency cutoff of the logic gates and is much faster than common synchronous operation limited to ~ 100 MHz.

We also investigate the behavior of a simple network consisting of an excitable system with self-feedback with time delay τ (Fig. 3a), *i.e.*, $V_{in}(t) = V_{out}(t - \tau)$ [29]. The time delay accounts for non-instantaneous transmission times along network links (for example, the propagation time along nerve cells connecting different areas of the brain [5]).

The delayed feedback link is realized as shown in Fig. 3b with $n_{\tau} = 40$ cascaded pairs of inverter gates, each imposing its propagation delay to the path, leading to a total time delay of $\tau = (21.3 \pm 0.5)$ ns, as characterized in Fig. 1b. The delayed feedback signal and an initial stimulus are both applied to the excitable node. As an excitable node has only one input, an OR gate is used to combine the two signals. The OR operation allows both signals to excite the node, but also other logic gate operations to combine inputs are possible, as discussed later. Here, the system is operated in its excitable regime.

When no initial stimulus is applied, the feedback system rests in a stable quiescent state. But, when a pulse (with width (1.6 ± 0.1) ns) is injected once, the system generates a periodic pulse train as shown in Fig. 3c. Initializations with multiple pulses result in similar pulse trains with shorter periods.

The dynamics arise from the delayed feedback. When a pulse is generated by the system, it travels through the

delay line during τ . Then, it is input to the node to generate another output pulse after the processing time (system response time) h . Therefore, the period of the pulses is $T = \tau + h$ for this coupling scheme, which is confirmed by the experiment.

This behavior is reproduced for systems with parameters $n_{\text{ref}} = n_{\text{pulse}} = 1$ that have a shorter refractory period and small pulse widths (Fig. 3d) and for systems with parameters $n_{\text{ref}} = 20$ and $n_{\text{pulse}} = 4$ that have a longer refractory period (Fig. 3e). However, when the refractory period is increased further to $n_{\text{ref}} = 45 > n_{\tau} = 40$, i.e., $T_{\text{ref}} > \tau$, self-sustained pulsing dynamics are no longer solutions of the system (Fig. 3f). Instead, the system responds only to the initial stimulus and then stays in the quiescent state. When this first response is fed back after passing the delay line, the excitable node is still in the refractory phase and, therefore, cannot generate another output pulse.

Two delay-coupled excitable nodes. – In this section, we study a network of two delay-coupled excitable nodes with delayed feedback, as shown schematically in Fig. 4a. The coupling and feedback delays are denoted by $\tau_C^{(1,2)}$ and $\tau_K^{(1,2)}$, respectively.

Here, we are interested in the parameter regime of synchronization between the two nodes, as such states are found to be important in the brain. For example, they help to understand cognition and learning and also pathological conditions such as Parkinson’s disease [30].

The coupling scheme in Fig. 4a has already been studied with the FitzHugh-Nagumo model, and the parameter regimes where coherent oscillations appear and their period and phase have been found [9, 21, 31, 32]. These regimes form straight lines in the parameter space of the delay times, given by the following conditions. Without loss of generality, assume for the coupling delays $\tau_C^{(1)} = \tau_C^{(2)} = \tau_C$ [21]. First, consider the case that the feedback delays are also equal, $\tau_K^{(1)} = \tau_K^{(2)} = \tau_K$. Then, if $2\tau_C$ and τ_K are approximately commensurate, i.e.,

$$2\tau_C N_C \approx \tau_K N_K \text{ with integers } N_{C,K} \in \mathbb{N}, \quad (1)$$

the dynamics exhibits self-sustained coherent pulse trains with an inter-spike-interval (period) of

$$T = \tau_K / N_C = 2\tau_C / N_K, \quad (2)$$

and a relative phase between the two nodes of 0 or π , depending on N_K . More specifically, the oscillations are in-phase (anti-phase), if N_K is even (odd). Coherent spiking is expected even if the coupling delays differ from Eq. (1) by an amount on the order of the pulse width of the excitable system [21].

To test these results experimentally, we realize this coupling scheme with a setup shown in Fig. 4b. We use $n_{\tau,C}$ and $n_{\tau,K}$ pairs of inverter gates to create the delay lines for coupling and feedback satisfying $\tau_C^{(1)} \approx \tau_C^{(2)}$ and $\tau_K^{(1)} \approx \tau_K^{(2)}$, respectively; thus, the same number of

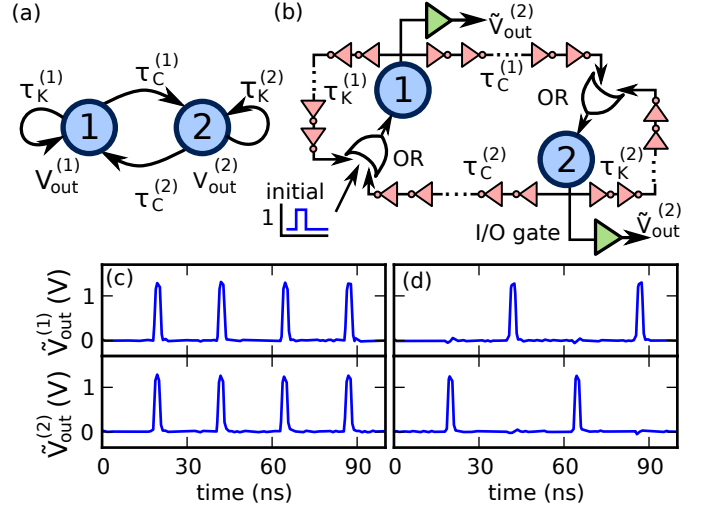


Fig. 4: (Color online) (a) Scheme of two excitable nodes with delayed mutual coupling and delayed feedback where delay links are represented as arrows. b) Representation with logic elements used for the coupling. The pink triangles with circles represent inverter gates that are incorporated in numbers $n_{\tau,C}$ and $n_{\tau,K}$ to adjust the delay times indicated on the links. Node parameters are $n_{\text{pulse}} = 4$ ($T_{\text{pulse}} = (2.1 \pm 0.2)$ ns) and $n_{\text{ref}} = 10$ ($T_{\text{ref}} = (5.3 \pm 0.2)$ ns). (c) Stable output of both nodes with coupling delays realized with $n_{\tau,C} = n_{\tau,K} = 40$ pairs of inverters leading to link delays $\tau_C^{(1)} = (21.6 \pm 0.2)$ ns, $\tau_C^{(2)} = (21.7 \pm 0.2)$ ns, $\tau_K^{(1)} = (21.6 \pm 0.2)$ ns, $\tau_K^{(2)} = (21.4 \pm 0.2)$ ns. (d) Same as (c) with $n_{\tau,C} = 40$, $\tau_C^{(1)} = (22.1 \pm 0.2)$ ns, $\tau_C^{(2)} = (21.2 \pm 0.2)$ ns, $n_{\tau,K} = 80$, $\tau_K^{(1)} = (43.0 \pm 0.4)$ ns, and $\tau_K^{(2)} = (43.5 \pm 0.4)$ ns. Electrical cross talk between the node outputs is visible as small oscillations near the noise floor. Additional logic gates are used to measure the link delays of this specific implementation.

inverter gates are employed in both cases. However, these delays are not exactly equal, because of heterogeneity in the logic gates’ propagation delays.

Furthermore, we use two- and three-input logic gates to combine the two delay lines and connections for external stimuli at the input of nodes. For that purpose, we use OR gates, so that any pulse at the input of this logic gate will be passed to the excitable node. However, for larger networks, an N -input logic gate that combines N inputs to an excitable node can be defined as desired using a 2^N -entry look-up table. This so-called synapse (when the excitable node is considered the soma of a silicon neuron) [13] allows for implementing inhibitory and excitatory connections and also to vary the coupling strength. The coupling strength is understood as the number of high inputs required for the “synapse” to pass on a pulse to the “soma” (excitable node).

This setup with delay lines and synapses as described above shows coherent spiking in Fig. 4c,d, when perturbed with a single pulse out of the quiescent state. The numeric values for the delays satisfy $\tau_C \approx \tau_K \approx 22$ ns ($N_C = 1$, $N_K = 2$) and $\tau_K \approx 2\tau_C \approx 44$ ns ($N_C = 1$, $N_K = 1$)

for Fig. 4c and d, respectively. With these two numerical values, we expect from Eq. (1) oscillations with period T of 22 ns and 44 ns, respectively. This behavior is found approximately in the experiment, where in-phase and anti-phase oscillations are seen with periods of $T = (23.0 \pm 0.2)$ ns and $T = (44.8 \pm 0.2)$ ns, respectively. For both sets of parameters, we observe small mismatch ($< 5\%$) between experiment and theory, likely due to the large processing time h .

Model. — In this section, we derive a Boolean map to describe the excitable node theoretically. In contrast to the experimental implementation, this model allows only for Boolean states, *i.e.*, $V \in \{V_{\text{high}}, V_{\text{low}}\}$, the low and high voltage of logic gates.

We model the three components of the setup (Fig. 1c), namely the AND gate and the two PGs, separately. First, we describe the AND gate with output signal $V_{\text{AND}}^{(j)}(t)$, where the superscript j denotes the nodes in the network. It is modeled by the map

$$V_{\text{AND}}^{(j)}(t + \Delta) = V_{\text{in}}^{(j)}(t) \wedge \neg V_{\text{ref}}^{(j)}(t), \quad (3)$$

where \wedge and \neg denote the Boolean AND and NOT operations, respectively, and Δ is the time step of the map. The NOT operation accounts for an inverted input to the AND gate, as shown in the setup. Second, the PGs denoted by n_{pulse} and n_{ref} in the setup are modeled by taking the flip-flop and the delay line combined with the XOR gate into account. The flip-flop creates events after a positive edge (PE) in $V_{\text{AND}}^{(j)}$. The delay line, together with the XOR gate, results in output pulses of the two PGs, *i.e.*, a high voltage for the time intervals $[s, s + T_{\text{pulse}}]$ and $[s, s + T_{\text{ref}}]$, respectively, after a PE in $V_{\text{AND}}^{(j)}$ at time s (denoted in the following as $V_{\text{AND}}^{(j)}(s) = \text{PE}$). Both, the flip-flop and the delay line combined with the XOR gate, are mathematically expressed as

$$V_{\text{out/ref}}^{(j)}(t) = \begin{cases} V_{\text{high}} & \text{if } \exists s \in (t - T_{\text{pulse/ref}}, t] : \\ & V_{\text{AND}}^{(j)}(s) = \text{PE} \\ V_{\text{low}} & \text{otherwise,} \end{cases} \quad (4)$$

for the two PGs denoted in the setup as n_{pulse} and n_{ref} , respectively. This description does not account for the processing time h of the flip-flop.

We model the three experiments in this paper with a time step $\Delta = 0.01$ ns. For the first experiment of one excitable node with constant input, we set $V_{\text{in}} = V_{\text{high}}$ in the model, which results in dynamics shown in Fig. 5a. The second experiment with delayed feedback of a single node is modeled with $V_{\text{in}}(t) = V_{\text{out}}(t - \tau)$ (Fig. 5b). Due to the delayed feedback, our theoretical description is a Boolean delay equation [20], which requires an initial history function for initialization. Here, we initialize $V_{\text{in}}(t)$ with a pulse on the interval $[-\tau, 0]$. Finally, the third experiment is modeled in Fig. 5c with $V_{\text{in}}^{(1)}(t) = (V_{\text{out}}^{(1)}(t - \tau_K) \vee V_{\text{out}}^{(2)}(t - \tau_C))$ and $V_{\text{in}}^{(2)}(t) = (V_{\text{out}}^{(2)}(t - \tau_K) \vee V_{\text{out}}^{(1)}(t - \tau_C))$, where \vee

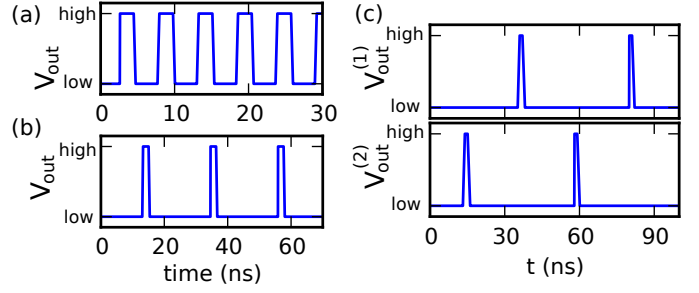


Fig. 5: (Color online) Simulation of Boolean map for $T_{\text{pulse}} = 2.1$ ns, $T_{\text{ref}} = 5.3$ ns. (a) Output of one node with constant stimulus, corresponding to Fig. 2b. (b) One node with delayed feedback, corresponding to Fig. 3c with $\tau = 21.3$ ns. (c) Two delay-coupled nodes with delayed feedback, corresponding to Fig. 4d with delays $\tau_C = 22$ ns, $\tau_K = 44$ ns.

indicates the OR operation. As above, we initialize the system with a pulse input to one excitable node.

The dynamics generated by the map is similar to the experiment in the overall picture, but in detail the waveforms differ, as the experiment shows imperfections, such as amplitude and timing noise and low-pass filtering effects. To capture these effects, we could use a model based on a set of delay differential equations with stochastic driving terms to describe all logic gates and propagation times in our setup, similar to Refs. [17–19].

Discussion. — Our excitable systems, designed in a bottom-up approach with autonomous Boolean circuits, display dynamics that are not as rich as for system designed in a top-down approach. For example, silicon neurons that are based on analog electronic components are known to show dynamics almost identical to biological neurons [13]. However, our approach allows for large networks, as it relies solely on logic gates. On the single FPGA used in this letter, there are enough logic gates to implement more than 10,000 interconnected excitable systems; but constraints on the wiring placement on the chip may decrease this number depending on the topology.

Furthermore, the logic gates and, hence, also our excitable system operate at time-scales on the order of nanoseconds, which is six to nine orders of magnitude faster than common silicon neurons that operate on a time scale of seconds, and a thousand times faster than the fastest so-called accelerated-time silicon neurons [13].

The fast time scales require us to implement links between excitable systems physically, thereby integrating both the network nodes and their connection on a single off-the-shelf reconfigurable electronic chip. This is another advantage over the VLSI approach (see Ref. [14]) where two chips are needed: a custom analog and a reconfigurable digital chip to implement the silicon neurons on the first and the wiring, the topology, on the latter. For the communication between both chips, an address-event representation is utilized, which leads to discretization errors in the coupling. By including the entire setup on an

FPGA and not using custom chips, our network realization becomes far less expensive than common approaches ($\sim \$300$) and excludes their discretization errors.

Artificial neural networks can be used for bio-inspired data-processing and machine learning. For this so-called reservoir computing, our network's simple spiking dynamics is suitable [22].

Conclusion. — We have proposed and built excitable nodes that are controllable in pulse width and refractory period. A single excitable node responds to a one-time stimulus with a single pulse and, when connected to a time-delayed network, our excitable nodes show self-sustained oscillations with phases and periods that are controlled by the coupling delays. This dynamics can be reproduced by a simple Boolean model and agrees quantitatively with theoretical studies based on FitzHugh-Nagumo models, indicating that our setup is suitable for fundamental studies on excitable networks.

As our setup relies exclusively on asynchronous logic gates and flip-flops, it is fully integrable on an inexpensive off-the-shelf FPGA, allows for thousands of nodes, and operates at speeds a thousand times faster than the fastest silicon neurons. Furthermore, it requires only little knowledge about electronic circuits, but mostly knowledge about a so-called hardware description language, which makes our experimental network science approach accessible for biologists and physicists. It will be invaluable as a test-bed for network science and might be applicable to ultra-fast neuro-inspired data processing.

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REFERENCES

- [1] IZHKEVICH E. M., *Dynamical Systems in Neuroscience* (MIT Press, Cambridge, MA) 2007.
- [2] STEINBOCK O., ZYKOV V. and MÜLLER S. C., *Nature*, **366** (1993) 322.
- [3] DAVIDENKO J. M., PERTSOV A. V., SALOMONSZ R., BAXTER W. and JALIFE J., *Nature*, **355** (1992) 349.
- [4] VARDI R., WALLACH A., KOPELOWITZ E., ABELES M., MAROM S. and KANTER I., *Europhys. Lett.*, **97** (2012) 066002.
- [5] KEENER J. P. and SNEYD J., *Mathematical physiology: Cellular physiology* Vol. 1 (Springer Verlag, New York, NY) 2009.
- [6] FITZHUGH R., *Bull. Math. Biol.*, **17** (1955) 257.
- [7] NAGUMO J., ARIMOTO S. and YOSHIKAWA S., *Proc. IRE*, **50** (1962) 2061.
- [8] DAHMS T., LEHNERT J. and SCHÖLL E., *Phys. Rev. E*, **86** (2012) 016202.
- [9] SCHÖLL E., HILLER G., HÖVEL P. and DAHLEM M. A., *Phil. Trans. R. Soc. A*, **367** (2009) 1079.
- [10] LEHNERT J., DAHMS T., HÖVEL P. and SCHÖLL E., *Europhys. Lett.*, **96** (2011) 60013.
- [11] KANTER I., KOPELOWITZ E., VARDI R., ZIGZAG M., KINZEL W., ABELES M. and COHEN D., *Europhys. Lett.*, **93** (2011) 66001.
- [12] VICENTE R., GOLLO L. L., MIRASSO C. R., FISCHER I. and GORDON P., *Proc. Natl. Acad. Sci. U.S.A.*, **105** (2008) 17157.
- [13] INDIVERI G., LINARES-BARRANCO B., HAMILTON T. J., VAN SCHAIK A., ETIENNE-CUMMINGS R., DELBRUCK T., LIU S. C., DUDEK P., HÄFLIGER P., RENAUD S., SCHEMMELE J., CAUWENBERGHS G., ARTHUR J., HYNNA K., FOLOWOSELE F., SAIGHI S., SERRANO-GOTARREDONA T., WIJEKON J., WANG Y. and BOAHEN K., *Front. Neurosci.*, **5** (2011) 73.
- [14] ARTHUR J. and BOAHEN K., *Learning in silicon: Timing is everything* in *Adv. Neur. Inf. Proc. Syst.*, edited by WEISS Y., SCHÖLKOPF B. and PLATT J., Vol. 18 (MIT Press, Cambridge, MA) 2006 pp. 75–82.
- [15] ZHANG R., DE S. CAVALCANTE H. L. D., GAO Z., GAUTHIER D. J., SOCOLAR J. E. S., ADAMS M. M. and LATHROP D. P., *Phys. Rev. E*, **80** (2009) 045202.
- [16] DE S. CAVALCANTE H. L. D., GAUTHIER D. J., SOCOLAR J. E. S. and ZHANG R., *Phil. Trans. R. Soc. A*, **368** (2010) 495.
- [17] MESTL T., BAGLEY R. J. and GLASS L., *Phys. Rev. Lett.*, **79** (1997) 653.
- [18] GLASS L. and HILL C., *Europhys. Lett.*, **41** (1998) 599.
- [19] EDWARDS R. and GLASS L., *Chaos*, **10** (2000) 691.
- [20] GHIL M. and MULLHAUPT A., *J. Stat. Phys.*, **41** (1985) 125.
- [21] PANCHUK A., ROSIN D. P., HÖVEL P. and SCHÖLL E., *Int. J. Bif. Chaos*, (2012) in print (arXiv:1206.0789).
- [22] SCHRAUWEN B., D'HAENE M., VERSTRAETEN D. and CAMPENHOUT J. V., *Neural Networks*, **21** (2008) 511.
- [23] JAEGER H. and HAAS H., *Science*, **304** (2004) 78.
- [24] MCCULLOCH W. S. and PITTS W., *Bull. Math. Biol.*, **5** (1943) 115.
- [25] JEONG Y., JUNG S. and LIU J., *A CMOS impulse generator for UWB wireless communication systems* in *proc. of Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on* Vol. 4 2004 pp. 129 – 132.
- [26] BURKITT A. N., *Biological Cybernetics*, **95** (2006) 1.
- [27] MAXFIELD C., *Design Warrior's Guide to FPGAs: Devices, Tools and Flows* (Newnes, Burlington, MA) 2004.
- [28] BELLIDO-DIAZ M. J., JUAN-CHICO J., ACOSTA A. J., VALENCIA M. and HUERTAS J. L., *Circuits, Devices and Systems, IEE Proceedings*, **147** (2000) 107.
- [29] FOSS J., LONGTIN A., MENSOUR B. and MILTON J., *Phys. Rev. Lett.*, **76** (1996) 708.
- [30] SCHIFF S. J., *Neural Control Engineering: The Emerging Intersection Between Control Theory and Neuroscience* (MIT Press, Cambridge, MA) 2011.
- [31] ERNST U., PAWELZIK K. and GEISEL T., *Phys. Rev. Lett.*, **74** (1995) 1570.
- [32] SHAYER L. and CAMPBELL S., *SIAM J. Appl. Math.*, **61** (2000) 673.